Patent claims

1. A photodiode arrangement having a photodiode and a submount, via which the photodiode is electrically contact-connected,

- the photodiode (1) having a metallization (12, 13) on the side facing the submount (2),
- the submount (2) having a metallization (22, 23) on the side facing the photodiode (1),
- the photodiode (1) and the submount (2) being connected to one another by means of eutectic bonding.

2. The arrangement as claimed in claim 1, characterized in that alignment marks are situated on the photodiode and/or the submount.

3. The arrangement as claimed in claim 1 or 2, characterized in that the photodiode (1) and/or the submount (2) are formed by a silicon chip.

4. The arrangement as claimed in at least one of claims 1 to 3, characterized in that the photodiode (1) and the submount (2) have a different outer contour and, accordingly, regions that protrude relative to one another.

5. The arrangement as claimed in claim 4, characterized in that contact pads (21) are situated on that region of the submount (2) which protrudes with respect to the photodiode (1), said contact pads being connected to the metallizations (22, 23) of the submount (2).

6. The arrangement as claimed in claim 4 or 5, characterized in that the optically active area (14) of the photodiode

is situated on that region of the photodiode (2) which protrudes with respect to the submount (2).

7. The arrangement as claimed in at least one of the preceding claims, characterized in that the metallization (12, 13) of the photodiode is a gold metallization and the metallization (22, 23) of the submount is a gold-tin metallization, or vice versa.

8. A method for producing a connection between a first semiconductor component and a second semiconductor component, in particular between a photodiode and a submount for a photodiode in accordance with the photodiode arrangement of claim 1, the semiconductor components connected to one another having a different outer contour,
characterized by the steps of
a) producing a multiplicity of first semiconductor components (1') on a first wafer (7),
i) producing a multiplicity of second semiconductor components (2') on a second wafer (8), in this case
j) providing a metallization (11') on the first semiconductor components of the first wafer (7),
k) providing a metallization (21') on the second semiconductor components of the second wafer (8),
l) forming trenches (9) in the first and/or the second semiconductor components, then
m) connecting the two wafers (7, 8) by eutectic bonding of the respective metallizations (11', 21'), the resulting wafer composite having a front side and a rear side, then
n) singulating the front side of the wafer composite in accordance with a first outer contour of the first semiconductor components to be singulated, only one wafer (8) being severed, and subsequently

o) singulating the rear side of the wafer composite in accordance with a second outer contour of the second semiconductor components to be singulated, only the other wafer (7) being severed.

9. The method as claimed in claim 8, characterized in that the wafer composite (7, 8) is turned between the two singulation steps.

10. The method as claimed in claim 8 or 9, characterized in that alignment marks are provided on the wafers.

11. The method as claimed in at least one of claims 8 to 10, characterized in that the end component singulated on both sides is released from the wafer composite and supplied to an automated apparatus for further processing.

12. The method as claimed in at least one of claims 8 to 10, characterized in that, during the eutectic bonding of the two wafers, a gold metallization of the first semiconductor components is connected to a gold-tin metallization of the second semiconductor components.

13. The method as claimed in at least one of claims 8 to 10, characterized in that the singulation is effected in each case by sawing.